

REMARKS

Claims 1, 20, and 24 have been amended. Claims 59-65 have been added. No new matter is included. Claims 1-37 are pending in this application.

Claims 1-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koizumi et al. (U.S. Patent No. 6,661,459) ("Koizumi") in view of Fossum et al. (U.S. Patent No. 5,055,900) ("Fossum"). The rejection is respectfully traversed.

Koizumi relates to a solid state image pickup device. Koizumi at col. 2, lines 60-63. Koizumi's device included a pixel having transistors, including transfer and reset transistors. Koizumi at col. 4, lines 16-30; FIG. 3. While Koizumi acknowledges that CCD sensors are known, Koizumi contrasts CCD sensors to Koizumi's sensor, which is a CMOS sensor (APS) as evidenced by the figures and description. Koizumi at col. 1, lines 12-66; col. 4, line 17 to col. 5, line 66; FIG. 3.

Fossum relates to a CCD sensor formed by first defining relatively deep trenches having relatively small lateral dimensions in the surface of a silicon bulk region. Fossum at col. 3, lines 3-27. Fossum teaches a p-type layer underlying an n-type layer and electrode layers for the capacitors formed in trenches that extend into the substrate to a depth above the p-type layer such that the junction between the junction between the p and n-type layers is within the depletion region when the device is biased. Fossum at col. 6, lines 16-25. According to Fossum, the electrodes serve to store charge. Storing and shifting charge requires the operation of four electrodes. Fossum at col. 6, lines 26-51.

The present invention relates to a pixel cell having a reduced potential barrier in a region where a gate and photodiode are in close proximity to one another. As amended, independent claim 1 recites, *inter alia*, "a gate of a transistor formed at least

partially below a surface of the substrate” and “a photo-conversion device formed adjacent to the gate, the photo-conversion device comprising a doped surface layer of a first conductivity type, and a doped region of a second conductivity type underlying the doped surface layer, wherein the doped surface layer is at least partially above a level of a bottom surface of the gate wherein the doped surface layer is at a level approximately between a level of a top surface of the gate and a level of the bottom surface of the gate, and wherein the second conductivity type layer is at a level below the level of the bottom surface of the gate.” Similarly, claim 20 recites, *inter alia*, “a gate of a transistor at least partially in the trench” and “a photo-conversion device formed adjacent to the trench, the photo-conversion device comprising a doped layer of a first conductivity type below the surface of the substrate, and a doped region of a second conductivity type underlying the doped layer of a first conductivity type, wherein the doped surface layer is at least partially above a level of a bottom surface of the trench, wherein the doped surface layer is at a level approximately between a level of a top surface of the gate and a level of the bottom surface of the gate, and wherein the second conductivity type layer is at a level below the level of the bottom surface of the gate.”

Both Koizumi and Fossum fail to teach or suggest these limitations. To overcome the deficiencies of Koizumi, which fails to teach or suggest any gate below a surface of the substrate or within a trench, the Examiner turns to Fossum. Fossum, however shows only capacitor gates, each formed within a trench and extending along a substrate surface outside the trench. Fossum fails to teach or suggest a “photo-conversion device comprising a doped layer of a first conductivity type below the surface of the substrate, and a doped region of a second conductivity type underlying the doped layer of a first conductivity type, wherein the doped surface layer is at least partially above a level of a bottom surface of the trench, wherein the doped surface layer is at a level approximately between a level of a top surface of the gate and a level

of the bottom surface of the gate, and wherein the second conductivity type layer is at a level below the level of the bottom surface of the gate.” Thus, the cited combination of Koizumi and Fossum do not teach or suggest the limitations of claims 1 and 20.

Additionally, one of ordinary skill in the art would not have been motivated to combine the teachings of Koizumi and Fossum in the manner suggested by the Examiner. The Examiner states that one of ordinary skill in the art would have been motivated to combine Koizumi and Fossum to “provide a longer path length for the photogeneration of carriers” and “to improve packing density.” Advisory Action dated May 18, 2005. Fossum clearly teaches that it is the depth of the storage region that increases photon absorption path length and allows for increased packing density. Fossum at col. 7, lines 10-14. Fossum teaches that a storage region is formed by applying a charge retention voltage to four electrodes and a charge repulsion voltage to an additional two electrodes. Since Fossum’s electrodes extend deep into the substrate, the storage region is deep.

In contrast, Koizumi teaches a CMOS sensor, or active pixel sensor (APS), having a transfer MOS transistor above the region between the photodiode and floating diffusion region. When the transfer transistor is in an off state, charge can be accumulated in the photodiode. When a voltage is applied to Koizumi’s transfer transistor gate, charge is transferred to the floating diffusion region. Koizumi at col. 5, lines 17-66. Thus, the transfer transistor is not operated to form a storage region, and is configured to operate differently than the capacitor electrodes in Fossum. The teachings of Fossum, therefore, are not interchangeable with those of Koizumi as suggested by the Examiner. There is nothing in these references to suggest combining their teachings. Thus, those of ordinary skill in the art would not have been motivated to combine the teachings of Koizumi and Fossum to achieve the claimed invention.

For at least the reasons set forth above as well as others, Applicants respectfully request the withdrawal of this rejection.

Claims 24-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koizumi in view of Fossum as applied to claims 1-23, and further in view of Furumiya et al. (U.S. Patent No. 6,639,293) ("Furumiya"). The rejection is respectfully traversed.

Like claims 1 and 20, as amended, independent claim 24 recites, *inter alia*, "a gate of a transistor formed at least partially below a surface of the substrate" and "a photo-conversion device formed adjacent to the gate, the photo-conversion device comprising a doped surface layer of a first conductivity type, and a doped region of a second conductivity type underlying the doped surface layer, wherein the doped surface layer is at least partially above a level of a bottom surface of the gate wherein the doped surface layer is at a level approximately between a level of a top surface of the gate and a level of the bottom surface of the gate, and wherein the second conductivity type layer is at a level below the level of the bottom surface of the gate." As set forth above, Koizumi and Fossum, even when considered in combination, fail to teach or suggest such limitations. Additionally, one of ordinary skill in the art would not have been motivated to combine Koizumi and Fossum.

Furumiya is cited, by the Office Action, for teaching an analog signal processor. However, Furumiya does not supplement the deficiencies of Koizumi and Fossum. For at least these reasons as well as others, Applicants respectfully request that the rejection be withdrawn and the claims allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Application No.: 10/602,721
Amendment dated May 26, 2005

Docket No.: M4065.0761/P761

Dated: May 26, 2005

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